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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,089	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In Claim 1 Lines 5-9, it is unclear as to whether the interrupt register is part of the status register or whether it is separate from the status register.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 6, 7, 9, 10, 13, 14, 17, 22, 23, 24, 27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,371,872 to Larsen et al. ("Larsen") and US Patent Number 6,499,078 to Beckert et al. ("Beckert").

5. In reference to Claim 1, Larsen teaches a plurality of first interrupts generated by a core (See Figures 1 and 2 Number 26 and Column 5 Lines 60-63); and a plurality of second interrupts that are generated external to said core (See Figures 1 and 2 Number 24 and Column 5 Lines 57-60). Larsen inherently includes a priority encoder, coupled to both said first interrupts and to said second interrupts, said priority encoder prioritizing said first and second pluralities of interrupts (See Figure 2 Number 28 and Column 5 Lines 63-65). Larsen does not teach that the plurality of first interrupts have programmable priorities; and a status register, coupled to said core, having a vector table, and an interrupt register, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities, said programmable priorities being different than those architected for said plurality of second interrupts. Beckert teaches an interrupt handler comprising a status register (See Figure 2 Number 40), having a vector table (See Figure 2 Number 50), and an interrupt register, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities, said programmable priorities being different than those architected for said plurality of second interrupts (See Figure 2 Number 48 and Column 3 Line 61 – Column 4 Line 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 1, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and

Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

6. In reference to Claim 2, Larsen and Beckert teach the limitations as applied to Claim 1 above. Larsen further teaches that said plurality of first interrupts comprise hardware interrupts and software interrupts (see Column 5 Lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 2, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

7. In reference to Claim 4, Larsen and Beckert teach the limitations as applied to Claim 1 above. Larsen further teaches that said core executes instructions (See Figure 1 and Column 5 Lines 30-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 4, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

8. In reference to Claim 5, Larsen and Beckert teach the limitations as applied to Claim 1 above. Larsen inherently includes an interrupt controller, coupled to said plurality of second interrupts, for providing said plurality of second interrupts to said priority encoder with predefined interrupt priorities (See Figure 1 and Column 5 Lines 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 5, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

9. In reference to Claim 6, Larsen and Beckert teach the limitations as applied to Claim 1 above. The priority encoder of Larsen will inherently produce an indication of which of said first and second pluralities of interrupts has the highest priority (See Column 5 Lines 63-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 6, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and

Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

10. In reference to Claim 7, Larsen and Beckert teach the limitations as applied to Claim 6 above. Beckert further teaches a vector generator, coupled to a priority encoder, for producing an interrupt vector corresponding to the interrupt having the highest priority (See Column 4 Lines 29-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 7, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

11. In reference to Claim 9, Larsen and Beckert teach the limitations as applied to Claim 1 above. Beckert further teaches that said configurable priority registers are writable by the processing system (See Column 3 Lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 9, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and

Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

12. In reference to Claim 10, Larsen teaches a microprocessor for handling interrupts, the microprocessor receiving firsts interrupts from an interrupt controller (See Column 5 Lines 57-60), the microprocessor comprising a core, for executing instructions, said core generating second interrupts (See Figure 1 and Column 5 Lines 30-54 and 60-63). Larsen inherently includes a priority encoder, coupled to said core, for receiving said first and second interrupts, said priority encoder prioritizing said first and second pluralities of interrupts (See Figure 2 Number 28 and Column 5 Lines 63-65). Larsen does not teach priority storage logic coupled to said core, for storing programmable priorities for said second interrupts, said programmable priorities being different than priorities for the first interrupts. Beckert teaches an interrupt controller having storage logic for storing programmable priorities for said second interrupts which are different than the priorities for the first interrupts (See Figure 2 and Column 3 Line 61 – Column 4 Line 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 10, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

13. In reference to Claim 13, Larsen and Beckert teach the limitations as applied to Claim 10 above. The device of Larsen inherently comprises first instructions for handling the first interrupts and second instructions for handling the second interrupts. The device of Beckert inherently comprises instructions for storing said programmable priorities into said priority storage logic.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 13, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

14. In reference to Claim 14, Larsen and Beckert teach the limitations as applied to Claim 10 above. Larsen further teaches that said plurality of first interrupts comprise hardware interrupts and software interrupts (See Column 5 Lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 14, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

15. In reference to Claim 16, Larsen and Beckert teach the limitations as applied to Claim 10 above. Beckert further teaches a plurality of interrupt priority fields corresponding to on of said second interrupts (See Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 16, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

16. In reference to Claim 17, Larsen and Beckert teach the limitations as applied to Claim 16 above. Beckert further teaches that each of the priority fields has a 5-bit field, which includes a 4-bit field, for storing 32 distinct interrupt priorities, which includes 16 distinct interrupt priorities (See Figure 2 and Column 4 Lines 24-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 17, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

17. In reference to Claim 22, Larsen, and Beckert teach the limitations as applied to Claim 10 above. Larson further teaches that the interrupt controller prioritizes received interrupt signals according to known priority schemes (See Column 5 Lines 63-65), and therefore the priority encoder uses priorities for the first interrupts established by the interrupt controller when prioritizing the first and second interrupts.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 22, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

18. In reference to Claim 23, Larsen and Beckert teach the limitations as applied to Claim 10 above. The priority encoder of Larsen will inherently produce an indication of which of said first and second pluralities of interrupts has the highest priority (See Column 5 Lines 63-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 23, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

19. In reference to Claim 24, Larsen and Beckert teach the limitations as applied to Claim 23 above. Beckert further teaches a vector generator, coupled to a priority encoder, for producing an interrupt vector corresponding to the interrupt having the highest priority (See Column 4 Lines 29-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 24, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

20. In reference to Claim 27, Larsen teaches receiving off-core interrupts (See Figures 1 and 2 Number 26 and Column 5 Lines 57-60); and receiving on-core interrupts (See Figures 1 and 2 and Number 24 and Column 5 Lines 60-63). Larsen inherently teaches sorting the received off-core and on-core interrupts according to their priority levels and producing an indication of which of the received off-core and on-core interrupts has the highest priority (See Column 5 Lines 63-65). Larsen does not teach that the on-core interrupts have programmable priority levels which are intermediate to the priority levels for the off-core interrupts. Beckert teaches an interrupt controller allowing the priority levels of interrupts to be assigned values intermediate to the priority levels of other interrupts (See Figure 2 and Column 3 Line 61 – Column 4 Line 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 27, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

21. In reference to Claim 29, Larsen and Beckert teach the limitations as applied to Claim 27 above. Larsen further teaches that the off-core interrupts are initially prioritized by an interrupt controller (See Column 5 Lines 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 29, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

22. In reference to Claim 30, Larsen and Beckert teach the limitations as applied to Claim 27 above. Larsen further teaches examining the priority levels of each of the received off-core interrupts, examining the priority levels of each of the received on-core interrupts, and selecting one of the received on-core or off-core interrupts with the highest priority level (See Column 5 Lines 63-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Larsen with the interrupt handler of Beckert, resulting in the invention of Claim 30, because Larsen teaches and interrupt handler but is silent as to its construction (See Column 6 Liner 37-43 of Larsen) and Beckert teaches an interrupt handle that allows the user to program the interrupt priorities and servicing information as desired (See Column 3 Lines 1-9 of Beckert).

23. Claims 3, 15, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen and Beckert as applied to Claims 2, 10, and 27 above, and further in view of US Patent Number 5,768,500 to Agrawal et al. ("Agrawal").

24. In reference to Claim 3, Larsen and Beckert teach the limitations as applied to Claim 1 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen and Beckert do not teach that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 3, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating

systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

25. In reference to Claim 15, Larsen and Beckert teach the limitations as applied to Claim 10 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen and Beckert do not teach that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 15, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

26. In reference to Claim 28, Larsen and Beckert teach the limitations as applied to Claim 27 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen and Beckert do not teach that the on-core interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 28, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

27. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen and Beckert as applied to Claim 10 above, and further in view of US Patent Number 4,056,847 to Marcantonio ("Marcantonio").

28. In reference to Claim 11, Larsen and Beckert teach the limitations as applied to Claim 10 above. Larsen and Beckert do not teach that said interrupt controller receives a plurality of third interrupts, prioritizes, said third interrupts, and provides the prioritized third interrupts to the microprocessor as first interrupts. Marcantonio teaches an interrupt controller that receives a plurality of inputs, prioritizes said inputs, and provides said prioritized inputs at an output (See Abstract and Column 2 Lines 5-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the priority encoder of Marcantonio, resulting in the invention of Claim 11, in order to provide a

means for producing a signal representative of the highest priority input of the received interrupts (See Column 2 Lines 10-15 of Marcantonio).

29. In reference to Claim 12, Larsen, Beckert, and Marcantonio teach the limitations as applied to Claim 11 above. Larsen further teaches that the first interrupts are presented to the microprocessor on first interrupt signal lines attached to the microprocessor (See Figure 1 Number 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the priority encoder of Marcantonio, resulting in the invention of Claim 12, in order to provide a means for producing a signal representative of the highest priority input of the received interrupts (See Column 2 Lines 10-15 of Marcantonio).

30. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen and Beckert as applied to Claim 10 above, and further in view of US Patent Number 5,148,544 to Cutler et al. ("Cutler").

31. In reference to Claim 18, Larsen and Beckert teach the limitations as applied to Claim 10 above. Larsen and Beckert do not teach that said priority storage means is located within a privileged resource within the microprocessor. Cutler teaches that a register for storing information related to an interrupt condition is accessible only during a privileged mode (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the privileged mode register access of Cutler, resulting in the invention of Claim 18, in order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

32. In reference to Claim 19, Larsen, Beckert, and Cutler teach the limitations as applied to Claim 18 above. Cutler further teaches that the privileged mode of operation during which the interrupt registers can be accessed is a kernel mode of operation (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the privileged (kernel) mode register access of Cutler, resulting in the invention of Claim 19, in order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

33. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen and Beckert as applied to Claim 10 above, and further in view of US Patent Number 4,110,822 to Porter et al. ("Porter").

34. In reference to Claim 20, Larsen and Beckert teach the limitations as applied to Claim 10 above. Larsen and Beckert do not teach that the first interrupts have eight

distinct priority levels. Porter teaches that interrupts may be assigned to one of eight priority levels (See Column 9 Lines 25-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the interrupt system having eight priority levels of Porter, resulting in the invention of Claim 20, in order to minimize the time required to answer an interrupt request by allowing a complete set of registers to exist for each level, and thus receipt of a higher priority interrupt does not require saving and restoring context data (See Column 9 Lines 25-38 of Porter).

35. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Beckert, and Porter as applied to Claim 20 above, and further in view of US Patent Number 4,402,042 to Guttag et al. ("Guttag").

36. In reference to Claim 21, Larsen, Beckert, and Porter teach the limitations as applied to Claim 20 above. Larsen, Beckert, and Porter do not teach that said second interrupts have at least nine distinct priority levels that overlap the priority levels for the first interrupts. Guttag teaches that a processor can have 16 interrupt levels that can be used for internal interrupts (See Column 34 Lines 1-9). Because Guttag and Porter both teach that Interrupt Level 0 is the highest priority and priority levels decrease as interrupt levels increase (See Column 34 Lines 3-4 of Guttag and Column 9 Lines 28-29 of Porter), the interrupt levels of Guttag overlap with the interrupt levels of Porter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Beckert, and Porter with the interrupt system having sixteen priority levels of Guttag, resulting in the invention of Claim 21, in order to reserve specific interrupt levels for the different internal interrupts (See Column 34 Lines 5-8 of Guttag).

37. Claims 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen and Beckert as applied to Claims 24 and 30 above, and further in view of US Patent Number 5,940,587 to Zimmer ("Zimmer").

38. In reference to Claim 25, Larsen and Beckert teach the limitations as applied to Claim 24 above. Larsen and Beckert do not teach programmable offset storage means, coupled to said vector generator, for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the programmable offset storage means of Zimmer, resulting in the invention of Claim 25, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment

of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

39. In reference to Claim 26, Larsen, Beckert, and Zimmer teach the limitations as applied to Claim 25 above. Zimmer further teaches that the interrupt vector table containing the offset values is created by a system executive, which is equivalent to kernel mode instructions (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the programmable offset storage means of Zimmer, resulting in the invention of Claim 26, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

40. In reference to Claim 31, Larsen and Beckert teach the limitations as applied to Claim 30 above. Marcantonio further teaches receiving the interrupt with the highest priority level (See Column 3 Lines 4-7). Larsen and Beckert do not teach examining a programmable offset; and calculating an interrupt vector for the one of the interrupts with the highest priority level utilizing said programmable offset. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector

generator to allow said vector generator to calculate said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the programmable offset storage means of Zimmer, resulting in the invention of Claim 31, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

41. In reference to Claim 32, Larsen, Beckert, and Zimmer teach the limitations as applied to Claim 31 above. The device of Zimmer inherently jumps to the interrupt vector in order to access the proper interrupt handler.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with the programmable offset storage means of Zimmer, resulting in the invention of Claim 32, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

Claim Rejections - 35 USC § 101

42. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 37, 38, and 39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 37, 38, and 39 recite the limitation "a computer data signal embodied in a transmission medium." The scope of this limitation encompasses both tangible and intangible transmission mediums.

Response to Arguments

43. Applicant's arguments with respect to claims 1-32 and 37-39 have been considered but are moot in view of the new ground(s) of rejection.

44. In response to Applicant's arguments concerning the rejection of Claims 37-39 under 35 USC §101, the limitation "a computer data signal embodied in a transmission medium" is recited. The scope of this limitation encompasses both tangible and intangible transmission mediums, and as such, the claims are non-statutory.

45. In response to Applicant's arguments that the programmable priorities, in which priorities or priority levels are being programmed, as claimed, is not the same as programmable assigning existing priorities to interrupts, it is noted that the features

upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It is unclear how the processor can respond to priority levels that were programmed at a later point and did not exist at the time the processor was created. Any priority level which the processor can respond to must have been architected into the processor to allow it to handle it, which would make it an existing priority.

46. In response to Applicant's arguments that Agrawal does not teach a performance counter interrupt, the Examiner notes that Agrawal teaches "a *counter* to periodically trigger an *interrupt* to track *performance* of a cache" [emphasis added] (See Column 8 Lines 34-43 of Agrawal and Page 18 Line 13 of Applicant's Remarks).

Oath/Declaration

47. In response to Applicant's Remarks and Exhibits regarding the declaration, the Examiner notes that the supplemental declaration submitted as "Exhibit F" is not currently in the official record for the present application. Applicant is requested to resubmit the supplemental declaration so that it may be entered into the official record of the case.

Conclusion

48. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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